

TITLE 400G QSFP-DD SR8 Transceiver	DOC No. RFD-20240223010-001	
	REVISION : 02	AUTHORIZED BY : Andy Yang
	DATE : 2024.02.26	CLASSIFICATION : CONFIDENTIAL

1. PRODUCT FEATURES

- Hot Pluggable QSFP-DD Form Factor
- Case Temperature Range of 0°C to +70°C
- Maximum Link Length of 100m on OM4 Fiber with KP4 FEC
- Single +3.3V Power Supply
- Power Dissipation < 10W
- Operating Case Temperature Options: - Commercial: 0 to +70°C
- RoHS 6/6 Compliant
- MPO-16 APC Connector

2. PRODUCT DESCRIPTION

2.1 PRODUCT NAME AND SERIES NUMBER(S)

QSFP-DD SR8 Active Optical Cable

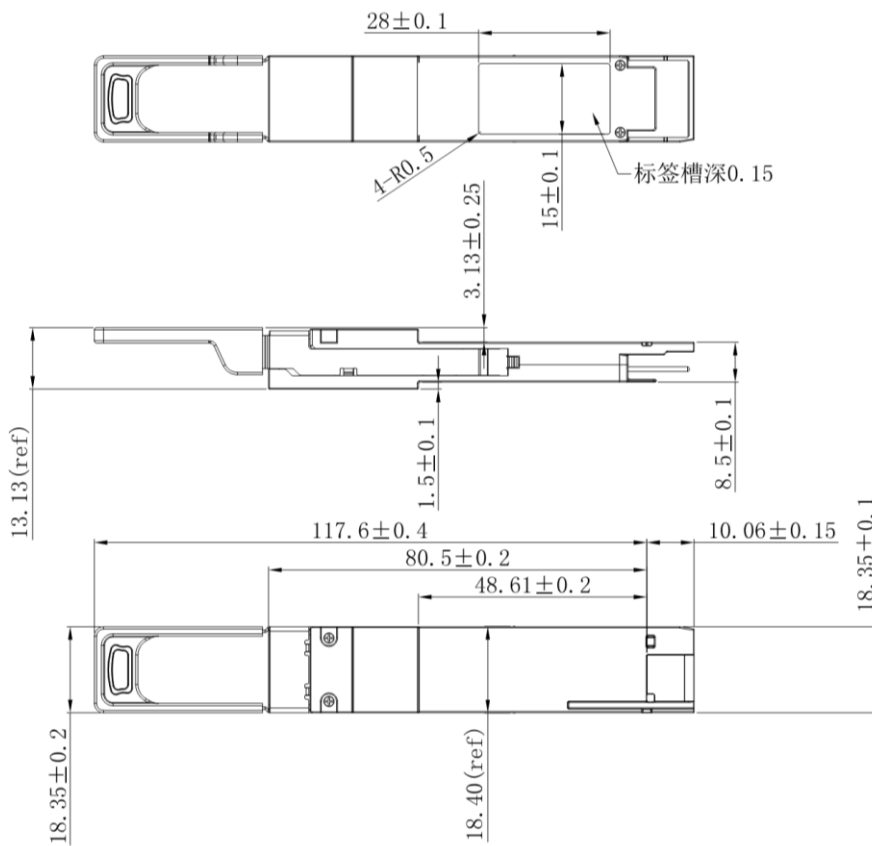
Data Rate	Wavelength (nm)	Distance	Media	DDMI	Connector	Temp.
425G	850	100 m	MMF	YES	MPO 1x16 APC	C

1. OM4 Fiber, 70m for OM3 Fiber, with KP4 FEC

2. Case Temperature

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2.2 DIMENSIONS, MATERIALS, PLATINGS AND MARKING



3. APPLICABLE DOCUMENTS AND SPECIFICATIONS

- 400G 100m on OM4 with FEC

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4. Absolute Maximum Ratings & Recommended Operating Conditions

Absolute Maximum Ratings				
Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	TS	-40	+85	°C
Supply Voltage	VCC3	-0.5	+3.6	V
Operating Humidity (Non-condensing)	RH	+5	+85	%
Receiver Damage Threshold per Lane	P _{RDMG}	+5	-	dBm

Recommended Operating Conditions					
Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Case Temperature(I-temp)	T _I	0	25	+70	°C
Power Supply Voltage	VCC3	3.1	3.3	3.5	V
Power Dissipation	P _d	-	-	10	W

Transceiver Electrical Characteristics						
Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Transmitter						
Signaling rate (each lane)	SR	26.5625 ± 100 ppm 100			GBd	-
Differential data input voltage per lane	V _{in,pp,diff}	900	-	-	mV	-
Differential termination mismatchal	-	-	-	10	%	-
Single-ended voltage tolerance range	-	-0.4	-	3.3	V	-
DC common mode voltage	-	-350	-	2850	mV	-

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Receiver						
Signaling rate (each lane)	SR	26.5625 ± 100 ppm			GBd	-
Differential output voltage	-	-	-	900	mV	-
Near-End ESMW (Eye Symmetry Mask Width)	-	0.265	-	-	UI	-
Near-End Eye Height, Differential (min)	-	70	-	-	mV	-
Far-End ESMW (Eye Symmetry Mask Width)	-	0.2	-	-	UI	-
Far-End Eye Height, Differential (min)	-	30	-	-	mV	-
Differential termination mismatch	-	-	-	10	%	-
Transition time (min, 20% to 80%)	-	9.5	-	-	Ps	-
DC common mode voltage	-	-350	-	2850	mV	-

Optical Characteristics						
Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Transmitter						
Signaling rate (each lane)	SR	26.5625 ± 100 ppm 100			GBd	-
Modulation Format	-	PAM4			-	-
Lane Wavelength	λ	840	850	860	nm	-
RMS Spectral Width	λ	-	-	0.6	nm	-
Average Launch Power, Each Lane	-	-6.5	-	4	dBm	-
Outer Optical Modulation Amplitude, Each Lane	-	-4.5	-	3	dBm	1
Launch Power IN oma Outer Minus TDECQ, Each Lane	-	-5.9	-	-	dBm	-
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), Each Lane	-	-	-	4.5	dB	-

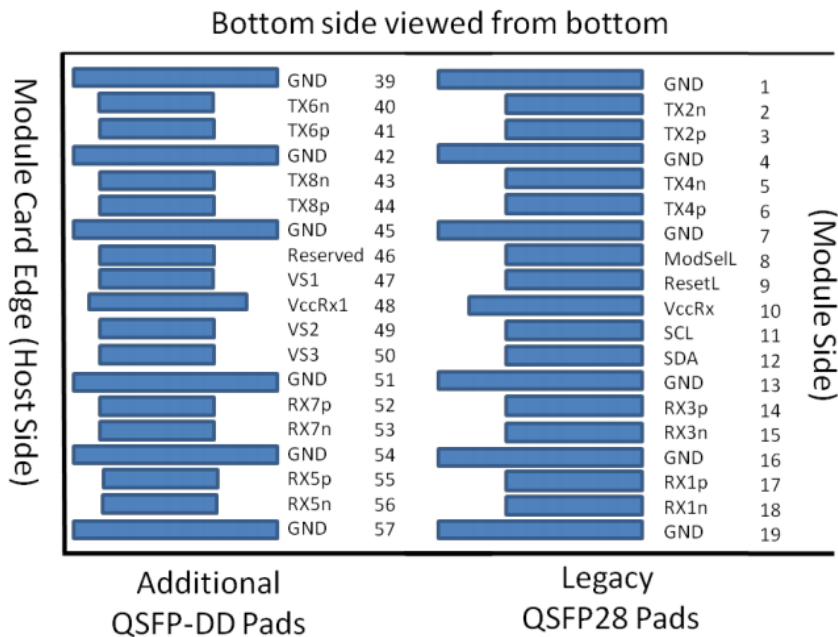
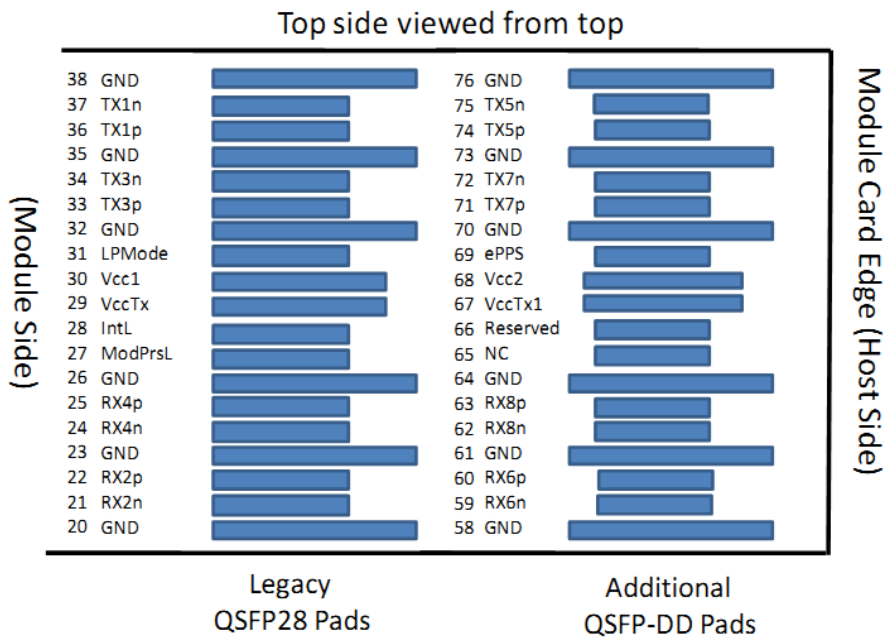
JESS-LINK PRODUCTS CO., LTD
PRODUCT SPECIFICATION

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Average Launch Power of OFF Transmitter	-	-	-	-30	dBm	-
Extinction Ratio	-	3	-	-	dB	-
Transmitter Transition Time, Each Lane	-	-	-	34	ps	-
Optical Return Loss Tolerance	-	-	-	12	dB	-
Receiver						
Signaling rate (each lane)	SR	26.5625 ± 100 ppm			GBd	-
Modulation Format	-	PAM4			-	-
Lane Wavelength	-	-	-	900	mVP-P	-
Damage Threshold, Each Lane	-	0.265	-	-	UI	-
Average Receive Power, Each Lane	-	70	-	-	mV	-
Receive Power (OMA Outer), Each Lane	-	0.2	-	-	UI	-
Receive Sensitivity (OMA Outer), Each Lane	-	30	-	-	mV	-
LOS Assert	-	-	-	10	%	-
LOS De-Assert	-	9.5	-	-	Ps	-
LOS Hysteresis	-	-350	-	2850	mV	-

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5. Pin-out Definition:



Pin Definitions

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Pin Assignment

Pad	Logic	Symbol	Description	Plug Sequence ⁴	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVC MOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVC MOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	LPMode	Low Power mode;	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1

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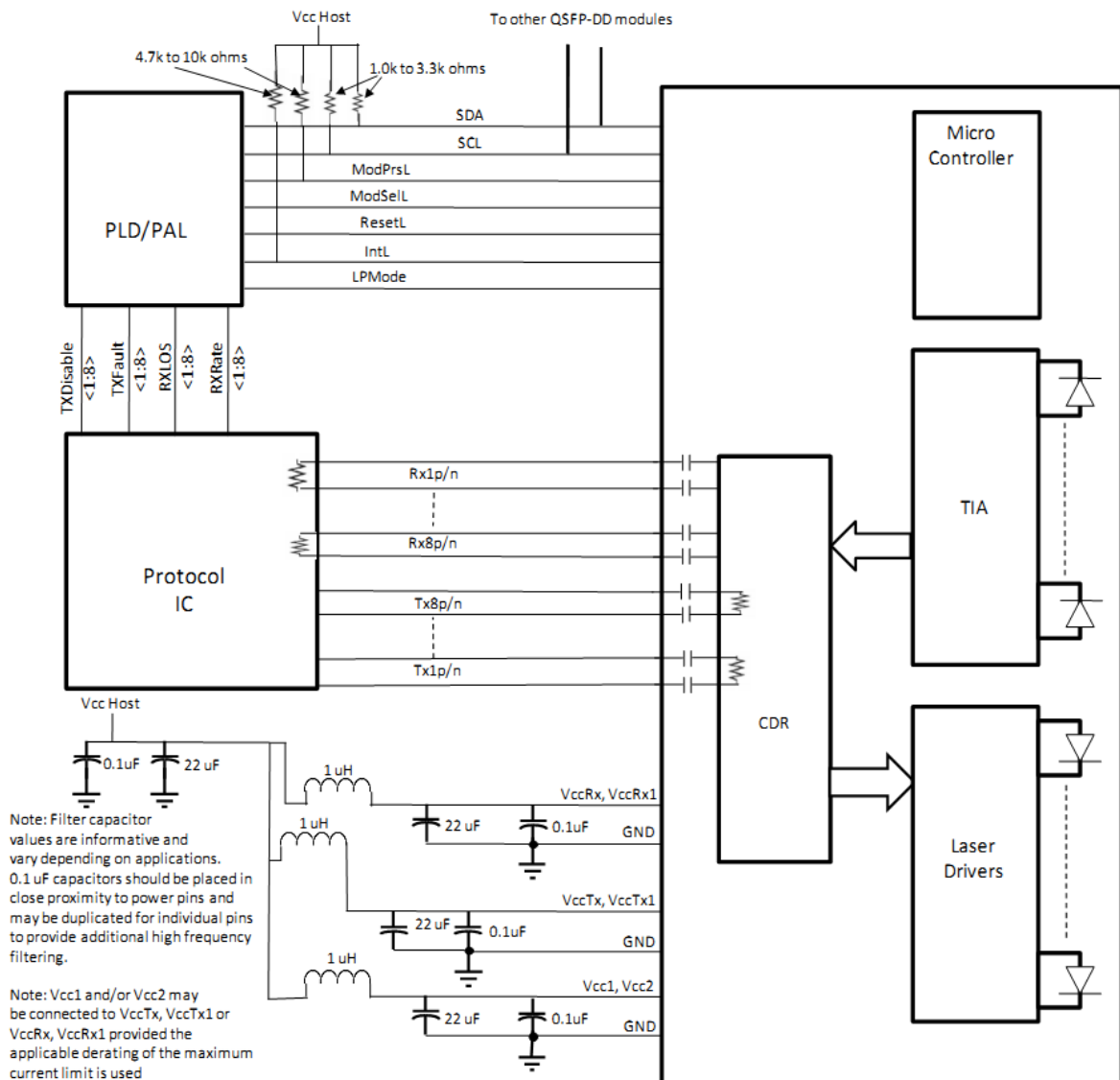
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LVTTL-I	ePPS	Precision Time Protocol (PTP) reference clock input	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Notes:

1. Circuit ground is internally isolated from chassis ground.

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Recommended Interface



QSFP-DD Optical Module

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Memory Map

Compatible with QSFP-DD CMIS rev 4.0.

Optical Interface Arrangement

The optical port is a male MPO connector receptacle, with fiber lane assignments as shown in Figure 3

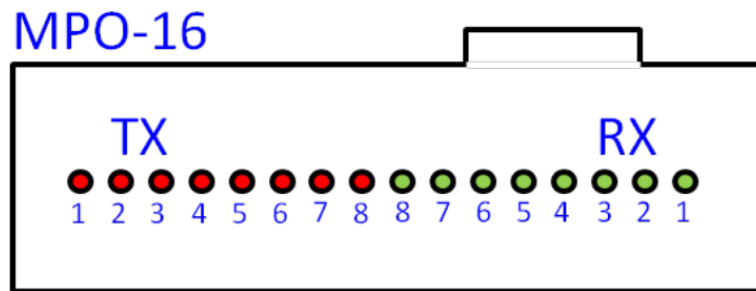


Figure 3, Optical interface arrangement. Lens upwards

Mechanical

SR8 QSFP-DD transceivers are compatible with the QSFP-DD Type 2 Specification for pluggable form factor modules.

6. Modification History

Rev.	Comments	Date	Originator	Approval
01	Preliminary Draft	2021.05.05	Albert Lin	Mike Sun
02	Dell PN	2024.02.26	Andy Yang	Mike Sun